Center for Embedded Networked Sensing

FPGA implementation of Crystal Compensated Crystal Timer

Interns: Carlos Gomez and David Haboud – Mentor: Young H. Cho

Special Acknowledgment to NESL team: Thomas Schmid, Jonathan Friedman, Zainul Charbiwala, Mani B. Srivastava

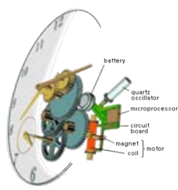
Problem Description: Unstable Clock Frequency over Changing Environment

Abstract

Time synchronization is an important service for networked and embedded systems. High quality timing information allows embedded network nodes to provide accurate timestamps, fast localization, efficient duty cycling schedules, and other essential functions. The first step in obtaining accurate time synchronization is to have highly stable source of clock. This project presents a new type of clocking source called Crystal Compensated Crystal Timer (XCXT) and its implementation using FPGA logic. The XCXT has timing stabilities similar to the timers based on temperature compensated crystal oscillators (TCXO) but has an implementation cost and power consumption that are on an order of magnitude less. We present our initial design of the XCXT using primitive components of Xilinx field programmable gate array (FPGA) and discuss the feasibility and expected result of the system. Our preliminary results indicate that our 8MHz XCXT can achieve ±1ppm timing stability using two inexpensive ±50ppm AT-cut quartz crystals with less than 160 four input look-up-tables (LUT4) and a single 18kbit block memory using Xilinx FPGAs.

Some wireless sensor network needs μseconds time difference from node to node at any given time

- Common oscillators used in current sensor nodes are inexpensive but unstable over operational temperature range
- Depending on the oscillator stability and the timing constraints, the rate of time synchronization has to be determined
- For example: In order to guarantee maximum frequency drift of 100μs using oscillator with ±100 ppm stability, the nodes must re-synchronize every 1 second.

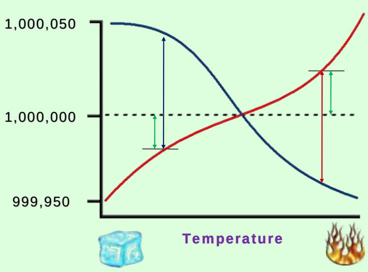


Device	Power	Stability	Price
32K Tuning Fork XO	<50uW	±25ppm	$0.50
8 MHz AT-cut Quartz XO	200uW	±25ppm	$0.50
32K DS32KHZ TCXO	750uW	±7.5ppm	$5.00
32K DS3232 TCXO	1mW	±2ppm	$7.00
10MHz DS4026 TCXO	6mW	±1ppm	$40.00
10MHz CO27VH15DE OCXO	1.5W	±0.2ppm	$250.00
8 MHz XCXT	1.4mW	±0.4ppm	$1.00

Problem Solution: Use the Frequency Difference between two Crystals to Compensate

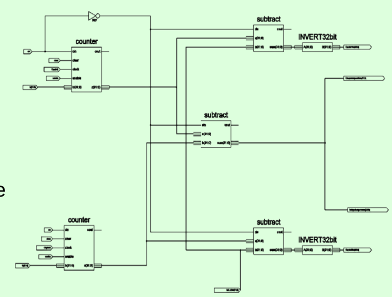
Research, design, and implementation of the XCXT on field programmable gate arrays (FPGA)

- The creation of the XCXT timer on FPGA requires knowledge of digital logic the use of schematic tools or VHDL code.
- High level design must be laid out before building the circuits on the CAD tools
- The schematic requires several different components to be made: Counters, Adders, Subtractors, and Ram Modules.
- The simulation must be done using the tools for the FPGA vendor.
- The waveforms are examined to verify the correct functionality of the XCXT design.



Differential Frequency Error Algorithm

- Using two inexpensive crystals
- Measure the cycle count over fixed period
- Take the difference in count between two crystals
- Determine the count difference between one of the crystal and the reference clock
- Record the differences in the count in the memory
- Compensate using the table in the memory



Problem Evaluation: Low Power and Low Cost Timer with Stability of TXCO and OCXO

Logic design and partial simulation of the XCXT system on FPGA tools and the expected result

- Tmote based prototype subjected to multiple temperature swings from -10°C to 60°C while compensating for the clock drift.
- Hardware logic equivalent of the algorithm designed in Xilinx ISE CAD tools
- Estimated FPGA resource usage comes to less than 150 basic 4-input look-up-tables (LUT4) and one 18bkit block memory
- Based on prototype result, we expect the similar mean stability of 0.47ppm with a sample standard deviation of 0.31ppm